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Future Prospects for Digital Optical Computing

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Future Prospects for Digital Optical Computing

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Features of optical bistability that are relevant to digital optical circuitry and possible architectures for such circuitry are described. Figures-of-merit are presented that indicate the material linear and nonlinear optical requirements for efficient optical switches.

Keywords: optical computing, optical bistability, optical interconnection, parallel image processing

1. INTRODUCTION

The concept of digital optical computing was discussed soon after the invention of the laser in 1960.[1] However, the nonlinear optical phenomena recognised during the early 1960s required power levels many orders of magnitude greater than demanded by a viable computing element, and were in any event unsuitable nonlinear responses for the implementation of memory and logic functions. It was in the late 1970s, when optical switches were demonstrated at milliwatt power levels, that serious consideration began to be given to the construction of prototype computing machines.[2] It must be emphasized that the circuitry discussed in this article, and the underlying devices, are still very much at the prototype stage. In order to produce competitive optical processors a number of enabling technologies must be developed. In addition the characteristics of the devices themselves must be improved. It is the need for optical switches of suitable power-speed combinations that provides a driving force in the search for new materials and structures exhibiting large nonlinear optical coefficients combined with relatively fast responses and having the capacity to be fabricated in the format of the selected computer architectures. There are prospects both for inorganic and for organic materials in this respect.

This article concentrates on *digital* optical information processing. The implication is that one wishes to work to high accuracy, with well defined optical parameters corresponding to logic levels zero and one, and with optical information signals that may be fanned-out to, or in from, only a few processing elements (in

order to maintain accuracies). The considerable effort that is also being put into analogue optical processing where global fan-out across image planes is used (e.g. Fourier processing[3]) and into threshold optics where discrete but high fan-out is used (e.g. associative memory processing[4]) will not be discussed. Furthermore special purpose (parallel) processors rather than general purpose computers will be given emphasis; the reason for this has to do with one particular advantage of optics over electronics: free-space interconnection with minimal crosstalk. It has been suggested that because the shortest duration pulses achieved to date are optical (down to 6 fs) and because of the femtosecond response times of certain nonlinear mechanisms, that one should be able to construct ultrafast optical switches for computing. Unfortunately, however, the power levels required in order to realise ultrafast gates must be extremely high. For a given available average optical power level, this means either that the switching repetition rate must be low or that very few gates can be operated simultaneously. In the former case there is no gain achieved by operating at high speed; in the second case the advantage of parallel interconnection is lost. For those tasks that do not demand high parallelism (small switching networks, perhaps cryptology) it may well be appropriate to attempt to replace electronic switches with faster optical devices, aiming at speed regardless of power-cost. More generally, however, it may be noted that over the history of computing the increases made in computational power have been achieved by an increase in parallelism as much as by an increase in gate speed.[5]

Electronic parallelism has reached values as high as 6×10^4 elements (the Connection Machine[6]) and will continue to grow. By comparison, whilst there may be 10^8 resolvable pixels/cm^2 at visible wavelengths, typical active device separations being discussed for 2-D arrays of optical switches are of order 10–100 μm. Hence the on-plane parallelism of optics is unlikely to be dramatically different from that of electronics. It is in the *combination* of parallelism and interconnects that optics does provide new features. The success of transistor electronics rests on the ease with which electronic charges interact via the Coulomb force. The same force is responsible for difficulties in electronic connections. It demands the use of wires with resulting cost of real estate on-chip, with crosstalk and with electromagnetic interference problems. In particular the number of pins off of a chip is typically one hundred and at best around three hundred. Optically, however, we envisage 10^4 or more logic gates on an "optical-chip" *each* interconnected to one or more gates on a subsequent chip. The interconnection would be in free-space or an alternative linear medium, using micro-optic imaging or holography. In principle an arbitrary, although fixed, interconnect pattern communicating between 2-D arrays of 10^4 elements is achievable using holographic optical elements. It is of course the absence of a photonic equivalent to the Coulomb force that enables the crosstalk and EMI-free propagation of multiple beams. A further aspect of optics, that is already being used in electronic machines, is data storage (read-only or erasable). One envisages optical storage in 2-D being used with simultaneous data acquisition to 2-D processor arrays, as opposed to the present, essentially sequential acquisition used in electronic machines. Thus one has a natural optical architecture involving 2-D images or data representations at all stages (acquisition, processing and interconnection) rather than a general purpose optical computer.

The above storage and interconnect concepts are most certainly going to be introduced into electronic machines. That is, optoelectronic integrated circuitry will be fabricated with detection at the gate level, interfaced with electronic processing and then with output optical modulators. The question that nonlinear optics research faces is whether the gates themselves can be replaced by "all-optical" devices, so avoiding the interfacing problems. In turn this requires an optical equivalent of the transistor or an invertor response and possibly the use of optical hysteretic responses. In addition the signal output levels from individual devices must be capable of acting as inputs to between one and ten further devices, this property is called cascadability and implies that each device must have an optical gain. The nonlinear interference filter family of devices described in section 2 of this article does have these properties, and existing devices allow the test-bed implementations described in section 3.

2. C.W. OPTICAL BISTABILITY

Semiconductor optical bistability, at cw (100 mW) power levels, was first reported in 1979.[1] Initial work, carried out using the small bandgap material InSb, required cryogenic operation, in the infrared spectral region, with a bulk material for which large (cm^2) uniform areas are difficult to fabricate. In contrast the design of narrow-band-pass ZnSe-based interference filters for visible operation proved successful and led to room temperature bistable operation in highly uniform material.[7] More recently work has also concentrated on liquid crystal devices,[8] and on GaAs multiple quantum well (SEED) devices.[9]

In order to illustrate a bistable system it is useful to consider the nonlinear Fabry-Perot interference filter (a medium sandwiched between partially reflecting mirrors). The qualitative characteristics are described by the simplified dynamic equation:

$$\frac{d\Delta}{dt} = \frac{\alpha D\, A\, I_0}{1 + F \sin^2(\phi_0 + b\Delta)} - \frac{\Delta}{\tau} \tag{1}$$

Δ refers to the material excitation; this may be a photogenerated carrier concentration as in the case of InSb, a temperature change as in the ZnSe filters, etc. The refractive index of the material is considered to be linearly dependent on the excitation level, leading to a phase shift across a given cavity of $\phi_0 + b\Delta$, where ϕ_0 is the phase shift at low irradiance levels. If the excitation level is itself linearly dependent on the internal irradiance I then the coefficient b is directly proportional to the effective nonlinear refractive coefficient:

$$n = n_0 + n_2 I, \tag{2}$$

and

$$b = \frac{2\pi\, n_2\, D}{\lambda_\nu\, \partial\Delta/\partial I}. \tag{3}$$

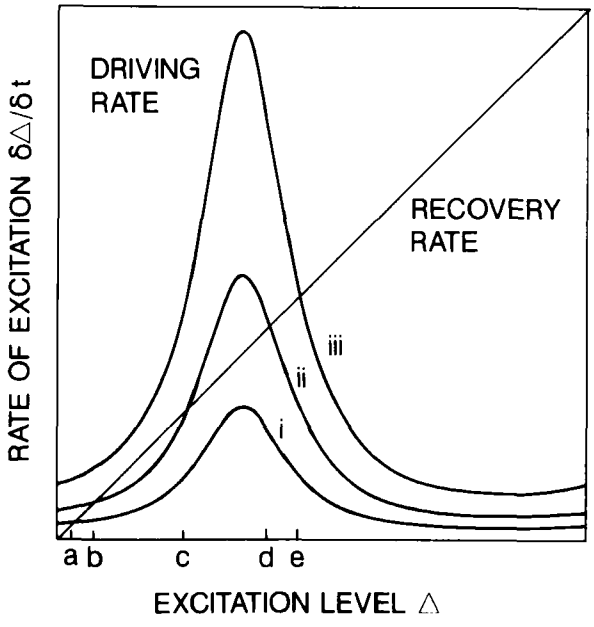


FIGURE 1 Graphical solutions for a nonlinear Fabry-Perot, showing terms for the rate of excitation production versus the level of excitation, see text and Equation (1).

D is the cavity thickness, α the linear absorption, λ_v the radiation vacuum wavelength. The cavity coefficients F and A in Equation (1) are determined by the absorption and the cavity mirror reflectivities. The excitation recovery rate is characterised by a fixed time τ in Equation (1). Figure 1 shows the two terms in the equation, plotted as a function of Δ, for three levels of the incident irradiance I_0 for a specific initial detuning ϕ_0. At the low and high I values (i and iii) there are single steady state solutions (intersections) for which the transmission into the cavity and the internal irradiance are self consistent with the optical phase generated by that irradiance. For the intermediate I_0 there are three steady-state solutions, the central one of which is unstable; this can be seen by considering a small fluctuation of Δ away from the intermediate solution. For an increase in Δ the (Airy function) excitation driving term exceeds the recovery (straight line) and Δ will increase with time, moving to the upper intersection, etc. Hence for a range of I_0 values one anticipates a pair of stable solutions—bistability. As ϕ_0 is altered the position of the Airy function peak occurs for different Δ values. A critical detuning ϕ_c and critical incident irradiance I_{0c} can be defined such that the excitation sink (load line) intercepts the driving curve at a tangent through the point of inflexion. For a Gaussian cw beam the corresponding power level is:

$$P_{oc} = \frac{\lambda_v}{2} \frac{\alpha r_0^2}{|n_2|} f, \tag{4}$$

f depends on the cavity parameters.[10] Figure 2 shows experimental examples of a cw-pumped ZnSe-based interference filter response, for different cavity detunings. In the upper, bistable trace switching occurs from the lower to upper bistable branch as one increases the incident power level and vice versa.

The dynamics of switching is also modelled by the graphical solution to Equation (1). Thus referring to Figure 1, for example, if I_0 is changed suddenly from level ii (with initial solution Δ_b) to level iii (final solution Δ_e), then the vertical difference between the Airy function (iii) and the load line indicates the rate of switching. This will be relatively slow initially but speeds up as Δ passes through the value at the peak, and then asymptotes to the steady state. The initial dynamics will be very slow if I_0 is raised only slightly above the switch point. This phenomenon is called critical-slowing-down and is shown in Figure 3 for a nonlinear Fabry-Perot

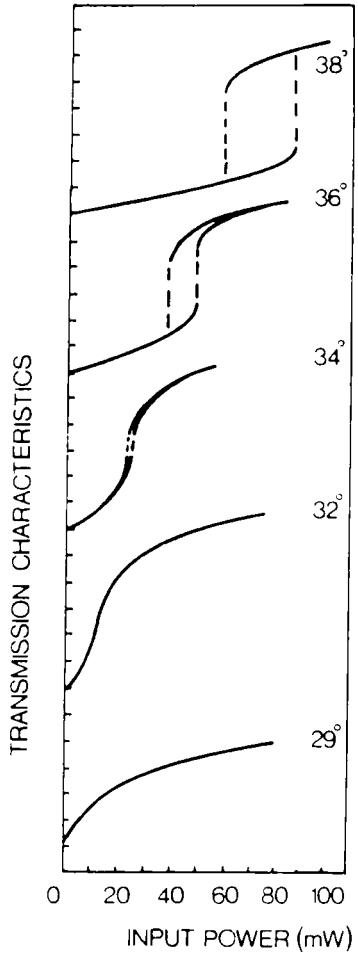


FIGURE 2 The family of optical responses of a nonlinear interference filter, showing nonlinear but monotonic output versus input for small initial detunings, through to a bistable response. Detuning is achieved by varying the angle of the incidence of the radiation to the ZnSe filter.[7]

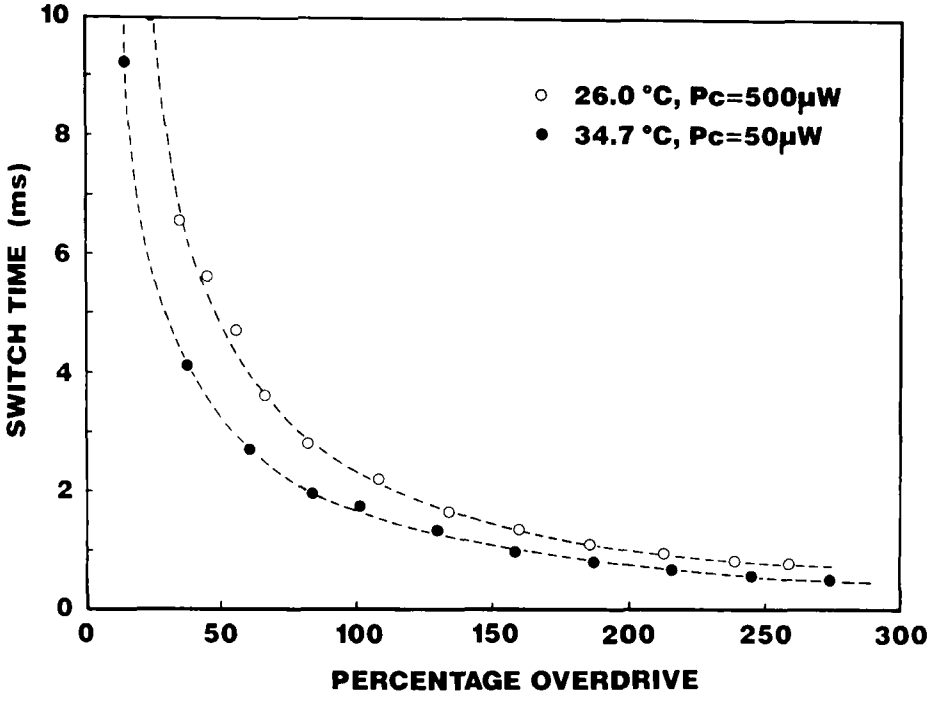


FIGURE 3 Switching time for a nonlinear etalon versus the percentage overdrive (the ratio of the incident power to the switch-up power) for a liquid crystal filled etalon.[8]

containing the nematic liquid crystal 4-cyano-4′-pentylbiphenyl. The switching time (away from the most critical regime) is characterised by the material recovery time τ.

It is now possible to see that one cannot achieve both low-power and fast switching simultaneously. Consider the mechanism for the nonlinear refractive index, n_2 is the index change per unit excitation density multiplied by the cw excitation level achieved for unit irradiance. However the latter level will be proportional both to α and to τ (the excitation removal rate). Hence from (4)

$$P_{oc} \propto \frac{\lambda_v r_0^2 f}{\tau \partial n/\partial \Delta}. \tag{5}$$

This result immediately points to the use of small volume samples and optimised cavities for a low power-time product. This product, the effective switching energy, has been typically nanojoule in most of the devices fabricated to date but is potentially sub-picojoule for optimised samples. Table I shows example experimental results for a range of materials, plus predicted parallelism and bit-rates.[11]

The remaining flexible parameter in $P_{oc}\tau$ is the index cross-section, $\partial n/\partial \Delta$. For electronic nonlinearities this is determined by transition oscillator strengths and by the proximity to resonance. Timescales for material recovery times range from

TABLE I

Example switching results for single element cw systems. The right-hand column is based on the assumption of 10 W cm^{-2} power dissipation over an array of devices.

	Area μm^2	Switch & Recovery μs	Power mW	Potential bit rate gate Hz/cm^2
InSb	700	0.25	0.6	10^{11}
ZnSe NLIF	20	10	4	10^9
Liq. Crystal	500	10^3	0.02	10^9
GaAs	75	0.02	4	10^{11}
SEED	10^3	0.03	2	10^{11}

Predicted[11] 10^4–10^6 parallelism, 10^{10}–10^{14} gate Hz/cm^2

femtosecond through to millisecond. The former refer to non-resonant electronic (virtual transition) nonlinearities, for which n_2 is related to the third-order nonlinear susceptibility

$$n_2 = 4\pi^2 \mathcal{R}e\ \chi^{(3)}/n^2c. \tag{6}$$

$\mathcal{R}e\ \chi^{(3)}$ values range from 10^{-8} to 10^{-16} esu. As one approaches resonance the real (long-term) excitation dominates and n_2, or an effective $\chi^{(3)}$, is definable only if the lifetime is independent of the level of excitation. For 1 μs carrier recombination in InSb $\chi^{(3)}$ values as high as 1 esu can occur. The long thermal recovery (diffusivity) time, for the temperature rise generated once the initial excitations have given their energy to the lattice, is responsible for the large effective index coefficients in thermal devices.

With respect to switching energies, the search for new nonlinear materials such as the organics is a search for large $\partial n/\partial\Delta$ values. For example, the 10 μW bistability achieved using nematic liquid crystals is due to the high thermo-optic coefficient at temperatures close to the nematic-to-isotropic phase-transition ($\partial n/\partial T$ can be as large as 0.1 K^{-1} under such circumstances, compared to typical semiconductor values of 10^{-4} K^{-1}). Alternatively one can define a figure-of-merit $|n_2|/\alpha\tau$ which should be maximised in optimal material. It is also necessary that the nonlinearity be maintained at the irradiance levels required, i.e. that it does not saturate. Quite generally for a bistable or switching device this leads to the requirement $\Delta n \approx \alpha\lambda_v$, where Δn is the total index change necessary for switching.

3. DIGITAL OPTICAL CIRCUITRY

Despite the relatively large switch energies of existing devices it has proven constructive to implement some basic optical circuits using them. These circuits have served as a focus to determine critical device parameters, to devise circuit architectures appropriate to optics, and to drive the optical interconnect technology that will be required for any optoelectronic parallel processors. In this section a series of circuits based on ZnSe filter technology is described. Circuits involving limited

numbers of information channels have been implemented. In the following architectures one must have in mind however arrays of 10^{-4}–10^{-6} parallel channels.

The use of a bistable response as a volatile memory is described first. Figure 4 demonstrates the use of transmission hysteresis as a temporary memory. A cw holding or bias beam is incident, bringing the transmission to the level "0" in the lower branch of the bistable loop (A). A *temporary* high switching signal increases the transmission from level A to level B; after the signal is removed the transmission drops but only slightly, to level C (the device latches from the lower to the upper bistable branch). A temporary reduction of the holding beam returns the transmission to A thereby resetting the latch. A low switching signal must be incapable of raising the total incident power above the switch level. Given the ability to hold close to the switch point then the bistable devices produce gain via the large signal difference between the zero and one output levels.

In 2-D parallel format a bistable plate therefore acts as a temporary memory or optical time-delay for a complete image, sustainable for as long as the array of hold beams (which has no information content) is maintained. To set up an iterative circuit capable of synchronising the flow of images, requires three or more bistable plates, Figure 4(b), with appropriately phased clocking of the holding beams.[12] Thus at the phase shown, with holding beam arrays on the left and right hand plates, a pre-processed image is stored by the right hand plate, it is processed in a non-latching logic-section of the circuit, and the processed image is captured and held (locked) by the left hand plate. The central plate acts as a shutter between the two images. By switching off the right hand bias array the pre-processed image is removed as is the immediate output of the processor. However the processed image is stored by the left hand plate for as long as its bias is maintained. The central plate can then be switched on in order to shunt the processed image through to the right hand plate. Continuing the clocking cycle enables information to flow around the circuit in such a way that processed images are prevented from contaminating the processing itself, by use of the buffered stores. Such a synchronous circuit has come to be called a 'lock-and-clock' architecture. Various modifications

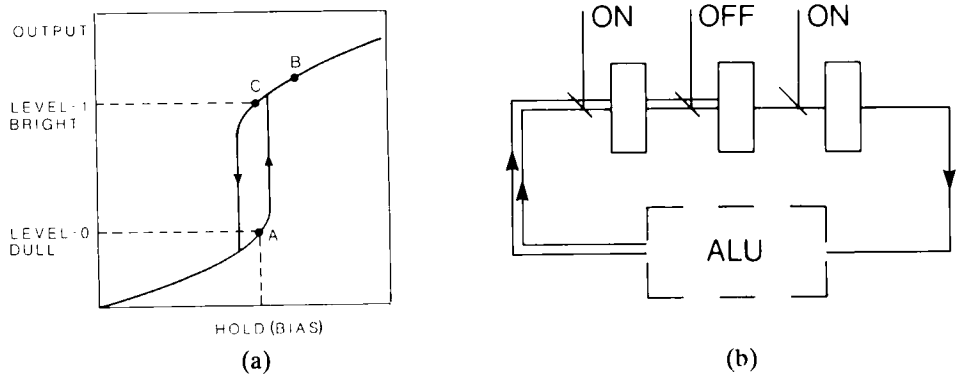


FIGURE 4 (a) Transmission response of an optically bistable plate, used as a latching memory. (b) Schematic of the "lock-and-clock" synchronous circuit.

are possible, involving latching logic, plates, operation in reflection, etc.[13] In parallel format the circuit corresponds to parallel shift registers with a wiring harness.

The use of bistable plates as temporary stores has the added bonus in that the output levels are both standardised and can be set to precisely the signal levels required of the processing, logic gates. Thus, the left hand plate of Figure 4(b) acts as a discriminator between low and high outputs of the processing unit. Its output must be cascadable through the following two plates and can, if necessary, be boosted to the required logic input signal levels. Thereby one achieves logic level restoration and the avoidance of error accumulation over multiple cycles.

As an alternative to bistable operation two non-hysteretic plates can be used to produce an R-S latching flip-flop by coupling the reflected (NOR) signal of each with the input to the other. A circuit with four independent R-S flip-flop channels has been operated.[14]

Whilst not essential to the image processing that is seen as the primary aim of a digital optical system, it is a challenge to optics to be able to perform numeric calculations. In turn this demands the ability to achieve binary full-addition. The simultaneously available transmission and reflection response of nonlinear filters proves to be ideally suited to this task, making possible the achivement, at a single pixel and on a single cycle, of the truth table that requires fourteen NOR-gates with four cycles. Whilst the demanded tolerance levels are finer for the single element device, its extreme simplicity may well lead to use in optical computation.[15] A single full-adder plate containing 10^4 active pixels in a circuit such as that of Figure 4(b) would be capable of 10^4 simultaneous additions of pairs of numbers presented in bit-plane format.

A version of an all-optical full-adder circuit has been implemented.[16] The reflected signal was itself propagated around a circuit employing a single temporary store, and used as one of the inputs to a further addition. In this way the implementation of restoring logic and of cascadability was again demonstrated as well as the ability to perform single-pixel, single-cycle addition.

Given parallel full-addition ability it is relatively straightforward conceptually to extend the architecture to achieve but-slice (or word-parallel) multiplication and, by incorporation of optical data reordering schemes such as the perfect shuffle, to implement such algorithms as the Fast Fourier Transform.

Using off-axis address, nonlinear interference filters give a hard limiting response which, under non-hysteretic conditions, is ideal for combinatorial logic. For example Figure 5 shows the bias beam reflection signal from a filter with an incorporated fully absorbing layer. As the signal beam level is altered the NOR/NAND logic function is achieved.

By using two, non-hysteretic, plates it has already been shown that the eight combinatorial functions that do not attempt to distinguish between the two inputs can be achieved by adjusting the holding beam levels.[17] If necessary all sixteen functions can be obtained by use of four logic plates. The point is that for a given functional unit in an optical circuit the processing logic at a given time (cycle) can be *programmed* by setting the holding beam levels. This would normally be a single instruction across the full image plane, but could include a measure of multiple instruction by setting different sections of a holding beam array at different levels.

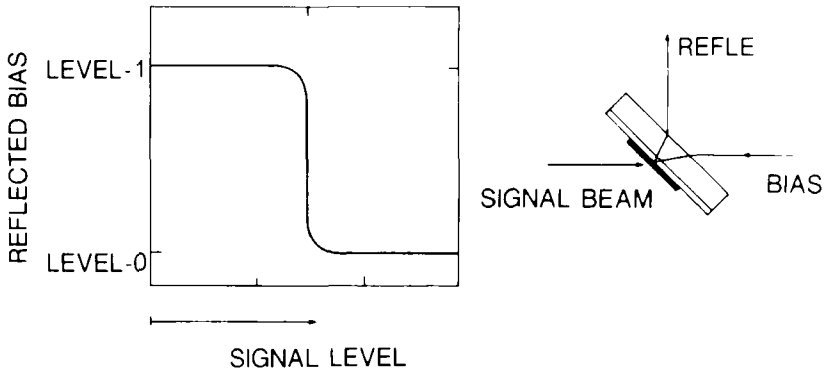


FIGURE 5 Hard-limiting achieved using the etalon design shown. A fully absorbing layer is placed onto the nonlinear etalon. The bias beam is incident through the glass substrate and the reflected bias forms the signal to the next device.

The programming would need to be carried out only at the 'slow' rate of the clocking.

The bit-slice addition circuitry described above consists of 2-D independent parallel pipelines in that there is no information exchange across any bit plane. There are no resulting fan-out restrictions, although the full-adder plate has 4-to-1 fan-in and places strong constraints on the contrast level of the preceding bistable plates.

Image processing algorithms, however, are most easily achieved using fan-out. This is demonstrated in the simplest manner by the process of binary edge extraction from a black-white image. Figure 6 examples one algorithm for the extraction, based on 1-to-5 fan-out from each pixel of the input image. Fan-out onto nearest neighbour pixels on a logic plate is pictured by the accompanying fan-in onto any single pixel. The fifth beam is directed to a second logic plate where it is fanned with the 4-input NAND response from plate 1. The following NAND, NOT functions complete the algorithm.

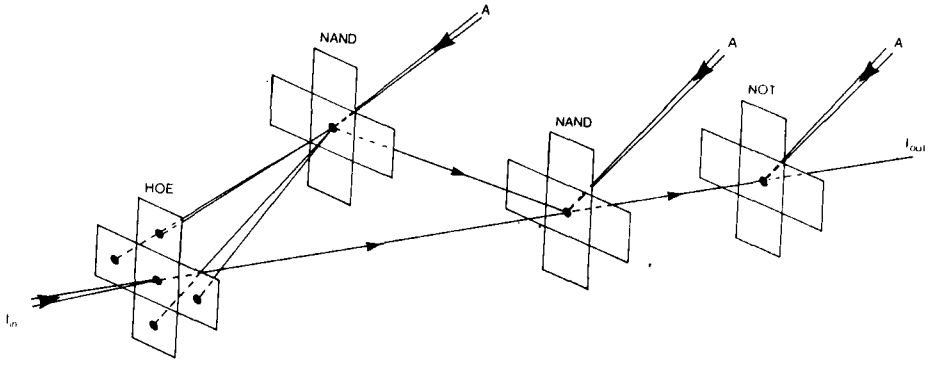


FIGURE 6 Elementary all-optical cellular logic image processor, using a pipelined architecture.

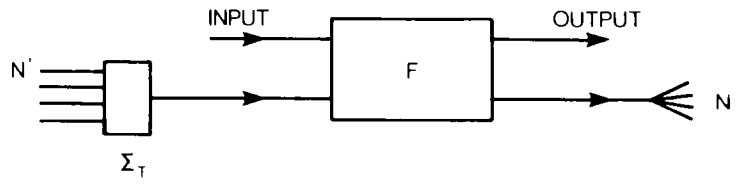
The fan-out itself is achieved with a holographic optical element in the circuit that has been constructed.[14] This set-up demonstrates the following features. (i) Identical logic plates are used for the three different logic functions, only the holding beam levels differ. (ii) The processing time is merely that required to 'switch' the sequence of three logic plates. This was achieved without using synchronisation but would require at least an initial bistable plate to hold an incoming image over the processing period.

Whilst edge-extraction only requires three sequential logic plates, any flexible pipelined processor would demand many more, perhaps with several input stages. A specialised system so constructed would be the most efficient in terms of throughput but it is more reasonable to suppose that processing time would be traded for power consumption, using a smaller logic sequence within an iterative circuit.

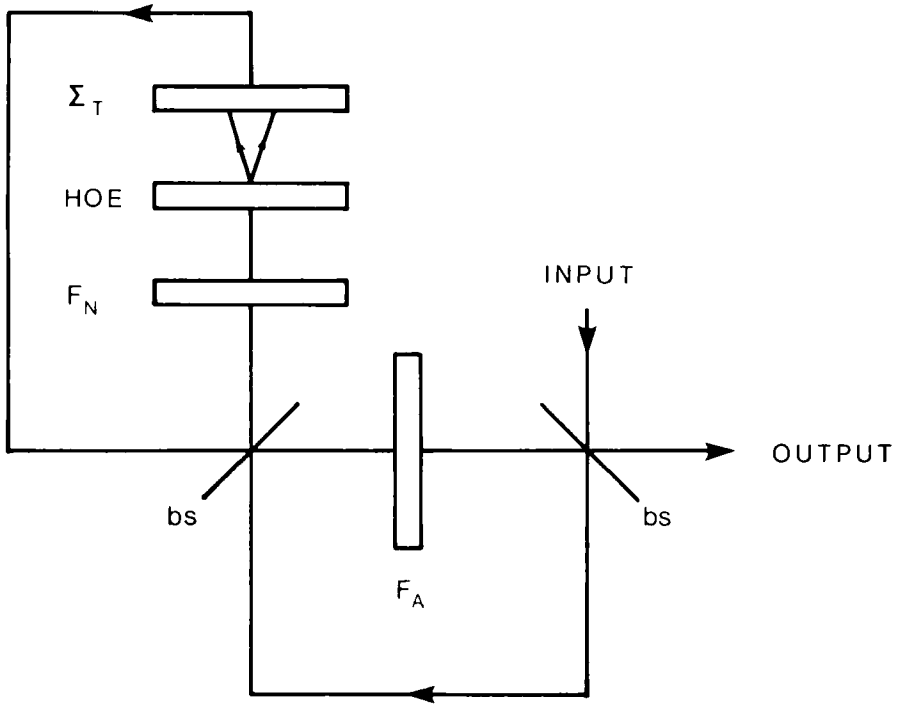
A number of iterative cellular processing schemes have been described, variously denoted by the acronyms OPALS,[18] DIAL,[19] DOCIP.[20] General algorithmic approaches are described by Binary Image Algebra and Symbolic Substitution.[21] The proposed and implemented experimental techniques tackle general computational problems through to highly specialised image processing. We recognise here a tradeoff between computational complexity and technological simplicity (in terms of the processing power of a given element, the parallelism and the number of cycles required for a given process). The architecture described below is designed to test the functions of nonlinear etalon devices within a circuit that can be made more flexible by the incorporation of further similar devices.

The combination of neighbour-correlation and circuit feedback is used electronically in cellular logic array processors. Figure 7(a) is a highly simplified version of one element in the early, CLIP-3 processor.[22] Each element contains two inputs to a function generator, F. One input is the ON/OFF value of the information at that element. The second input is a thresholded value of the, possibly weighted, sum (Σ_T) of outputs from the neighbouring function generators. Two inputs are taken from F, one is fanned out to each of the neighbours to produce part of their weighted sum. The second output can be considered to be the temporary output element of the calculation; it may also be fed back. F is pre-programmed to give any pair of the binary logic functions at the two outputs. Depending on the choice of functions a number of image processing operations are achievable; the output evolves to the processed version of the input image. For example image expansion or compression, noise removal or skeletonisation are achievable; also non-local processes such as joining of pixels and line recognition. A separate function circuit is required for each array cell.

A possible optical version of this simplified CLIP cell-array is shown in Figure 7(b). F_A, F_N are independent single-function generators; they could be the programmable optical devices. HOE is a fixed holographic optical element that produces, simultaneously at all image pixels, the required interconnect pattern. Σ_T is a multiple input AND gate that provides optical thresholding. A fixed input can be sustained throughout the processing as shown, or the evolving ouput could be fed back, having removed the input after the first cycle. Depending on the details of the system fan out/in of 1-to-4 or greater is required, although in principle the thresholding operation could be staged in order to reduce the cascadability de-



(a)



(b)

FIGURE 7 (a) Simplified electronic array processing element. (b) Optical implementation of an array processor, with elements equivalent to those of Figure 7(a).

mands. Three bistable plates in the iteration cycle would provide synchronisation if required. This is an example of the type of circuitry that is currently being constructed.

4. SUMMARY

Architectural features that form a potential basis for optical cellular logic image or numeric processing have been addressed. These include (i) the use of all-optical elements for logic and latching memory, (ii) the programming and clocking of the

machine via holding beam modulation in Single-Instruction-Multiple-Datastream fashion, and (iii) the use of holographic optical elements for beam array generation and for fan-out/in interconnects. Devices with minimal parallelism have been implemented as existence proofs of the above features. One requires however a number of enabling technology developments in order to achieve a viable level of parallelism for special purpose digital image processors. These technologies must include array and interconnect holography, solid-state lasers or laser arrays for efficient pump sources, sample reticulation, simultaneous 2-D data acquisition from read-write non-volatile optical storage (that does not require holding beam address to maintain memory) and/or SLM input devices. Further targets are the development of reconfigurable interconnects to enable flexibility in the ability of the architecture to complete algorithmic tasks in a minimum number of cycles, and efficient algorithms involving the non-local interconnection that optics can achieve simply where electronics has difficulties. Finally, the science underpinning the nonlinear elements themselves must be further understood in order to progress the drive towards improved all-optical switches and modulators.

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